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REMARKS

The indication of allowable subject matter in claims 17-20 and 23 is acknowledged and appreciated. In view of the following comments, it is respectfully submitted that all of the claims are patentable over the cited prior art.

The drawings are objected to for minor informalities. It is respectfully submitted that the enclosed amendment obviates the issues raised by the Examiner. Accordingly, it is respectfully requested that this objection be withdrawn.

Claims 12-16, 21 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Itakura '270 ("Itakura") in view of Nishitoba '186 ("Nishitoba"). Claim 12 is independent. This rejection is respectfully traversed for the following reasons.

The Examiner admits that Itakura does not disclose or suggest "a plurality of units of the first current distribution MISFET and the first current input MISFET are provided for the semiconductor chip, and wherein *a bias line connected to a gate electrode of the first MISFET and gate electrodes of the first current distribution MISFETs and shared by the gate electrodes is further provided*" (emphasis added). The Examiner therefore relies on the alleged current distribution MISFETs of Nishitoba and modifies Itakura by including the current distribution MISFETS of Nishitoba in an attempt to reach the claimed invention. Even assuming *arguendo* that the Examiner's interpretation of the cited prior art is proper, it is respectfully submitted that the Examiner's proposed combination is improper.

As expressly disclosed in col. 2, line 15 – col. 3, line 9 thereof, Itakura is specifically designed to address the deviation in ***threshold voltages*** of the diode-connected transistors in the

bias circuits to prevent differences in current consumption between the chips. According to this expressly stated objective, Itakura discloses arraying and integrating electronic circuits into a chip, where diode-connected input-side transistors are distributed in every circuit. Based on such a configuration, Itakura discloses that the average of deviations in the threshold voltages between the chips becomes almost equal, and expressly desires uniformly arranging a large number of transistors so as to reduce the deviation.

In this regard, Itakura discloses connecting the plurality of transistors parallel to each other and supplying voltage uniformly to each transistor. To effect such an arrangement, the transistors, to which drains and gates are connected, are arrayed in a chip and are connected to each other. Itakura expressly desires such a configuration to effect the disclosed objective. That is, the disclosed structural arrangement is required to supply gate voltage uniformly with reduced deviation between the chips, which voltage (gate voltage of diode-connected transistors) is used to connect the gates of the current output-side transistors.

In direct contrast, the present invention is directed to ***current distribution*** and is wholly unrelated to the structural configuration of Itakura related to ***voltage distribution***. Indeed, any attempt to modify Itakura by incorporating the teachings of Nishitoba would render Itakura inoperable for its intended purpose. That is, as noted above, the disclosed purpose of Itakura is based on a structure which arrays the diode-connected transistors in each chip and connects said transistors to each other. However, if current distribution transistors are included into the device of Itakura, the disclosed connections and arrangement of the circuit of Itakura would be undone, whereby the disclosed purpose of reducing voltage deviation would be reversed.

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The Examiner is directed to MPEP § 2143.01 under the heading "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE"

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

In the instant case, it is respectfully submitted that the proposed modification of Itakura with the teachings of Nishitoba would render Itakura inoperable for its intended purpose of reducing voltage deviation, so that "there is no suggestion or motivation to make the proposed modification." In this regard, Itakura teaches away from the proposed modification.

It should be noted that the present invention is directed to the ***combination*** of a current distribution MISFET circuit designed to make it possible to supply the same amount of current to each current supply section. Itakura, on the other hand, is directed to the combination for supplying uniform voltages to each transistor. Accordingly, the entire purpose and intended operation of Itakura would be destroyed if a current distribution MISFET were to be included because the expressly desired arrangement of transistors would be disassembled. In this regard, the cited prior art is completely silent as to the issues related to current distribution in the particularly referenced circuit arrangement of the present invention, and therefore provides no motivation for incorporating the current distribution MISFET in the specific arrangement set forth in claim 12.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 12 is patentable for the reasons

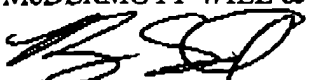
set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
McDERMOTT WILL & EMERY LLP



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